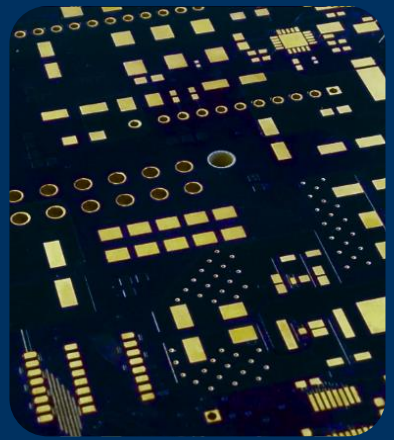


SPISimPro

Fully integrated signal, power integrity analysis suite

SPISim

EDA expertise in Signal, Power Integrity and Simulation

EDA focusing on SI and PI:

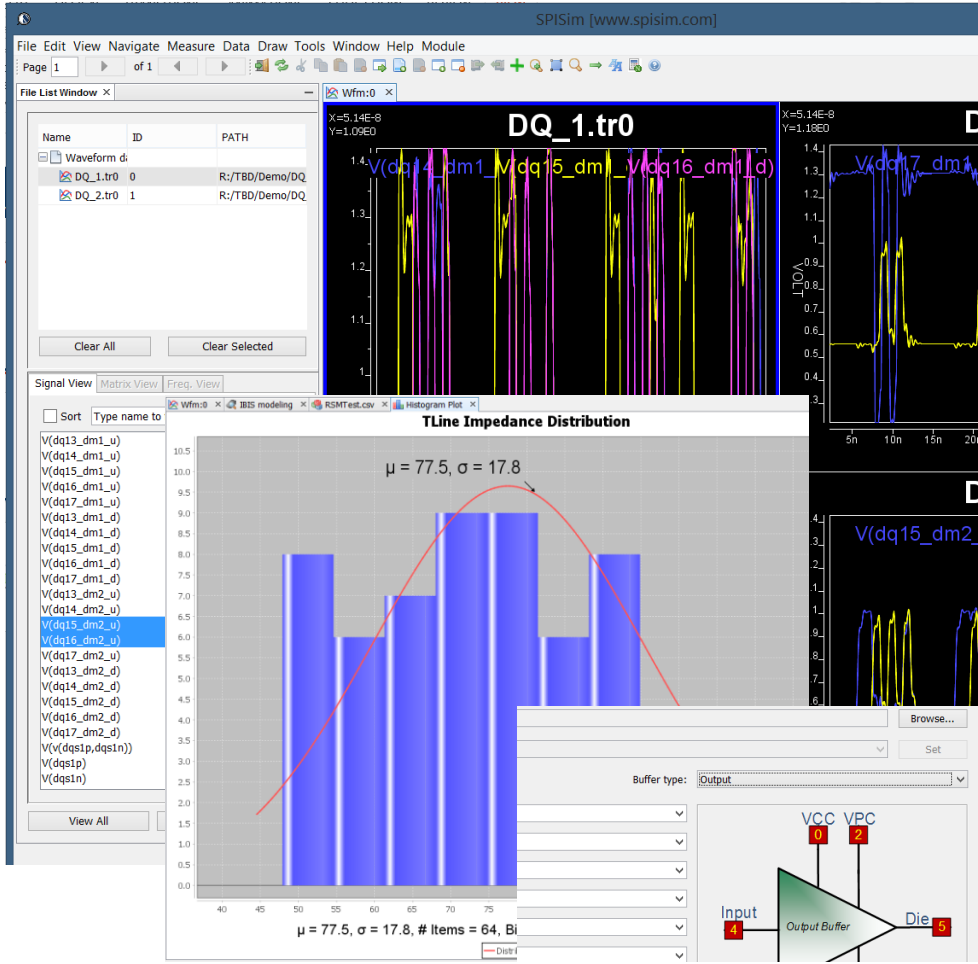
SPISim is an EDA company specialized in system level signal, power integrity and simulation. From pre-layout schematic editor, IBIS, Verilog-A, transmission line and S-parameters modeling and analysis to post-layout net based performance analysis and design synthesis. From design-of-experiments setup, design sample generations to linear programming, neural network or genetic algorithm based optimization. We have experience in them all and can provide industry level best practice flow to meet your high speed system design needs.

Unified analysis suite:

SPISim brings latest software technologies in framework infrastructure and libraries to our design. These modules and integrated suite are built from ground up to meet SI/PI engineers' day-to-day needs. Be they TD/FD/TLine/S-Parameters focused waveform viewing, model generation and analysis, or IBIS inspector and tuning capabilities, you will not find such comprehensive SI/PI capabilities in our single analysis suite.

Powerful yet affordable:

All our tools are cross-platform (Windows, Linux and OSX), self-patchable and extra licenses free. That means no need for hassle MCR installation or additional toolbox's purchase. Our tools can also integrate with your existing highly priced point tools to compose a streamlined flow. We also provide customization service based on our modules. With this, your company can focus on core business logic instead of reinventing wheel for the design infrastructure.



SPISimPro

A complete analysis suite

Our flag ship product:

SPISimPro is our flag ship product for complete SI/PI analysis capabilities. It has complete pre-layout and post-layout related modules fully integrated in a single comprehensive and streamlined UI.

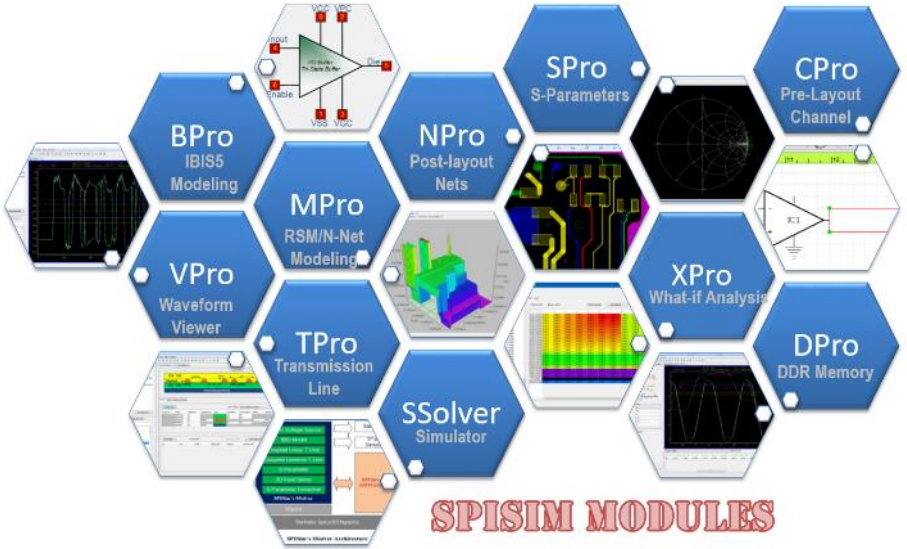
Pre-layout analysis from A to Z:

SPISimPro suite integrated the following core modules for pre-layout modeling and analysis needs:

- NPro: Post-layout design viewer with net traversal focused. Extract nets as spice netlist or schematic for CPro.
- CPro: Schematic channel builder supporting either free form channel design or extracted nets from Npro. Simulate interactively or perform what-if analysis.
- VPro: a powerful FD/TD waveform viewer and analyzer w/ signal generator;
- SPro: S-parameter analysis and automation;
- TPro: Layer stack-up and Transmission line modeling and analysis;
- MPro: RSM, DOE, ANN, GA or Linear programming based modeling and optimization;
- BPro: IBIS model inspector, spec., design and simulation based behavioral model generation;
- DPro: DDR time domain simulation processing for JEDEC parameter reporting.

Dynamic and Scalable:

Modules used in SPISimPro complete suite are plug-N-play and can be extended to meet your growing designs and technology challenges. Add-ons can also be developed for your organization for to present a step-by-step, check mark or wizard based analysis flow.



NPro:

Post-layout design reviewer and net extractor

Post-layout design review:

SPINPro accepts MCM/BRD, ODB++ and SPD files. Design is then presented to user for design review or simple mock-up. Final design can be saved as SPD or ODB++ files.

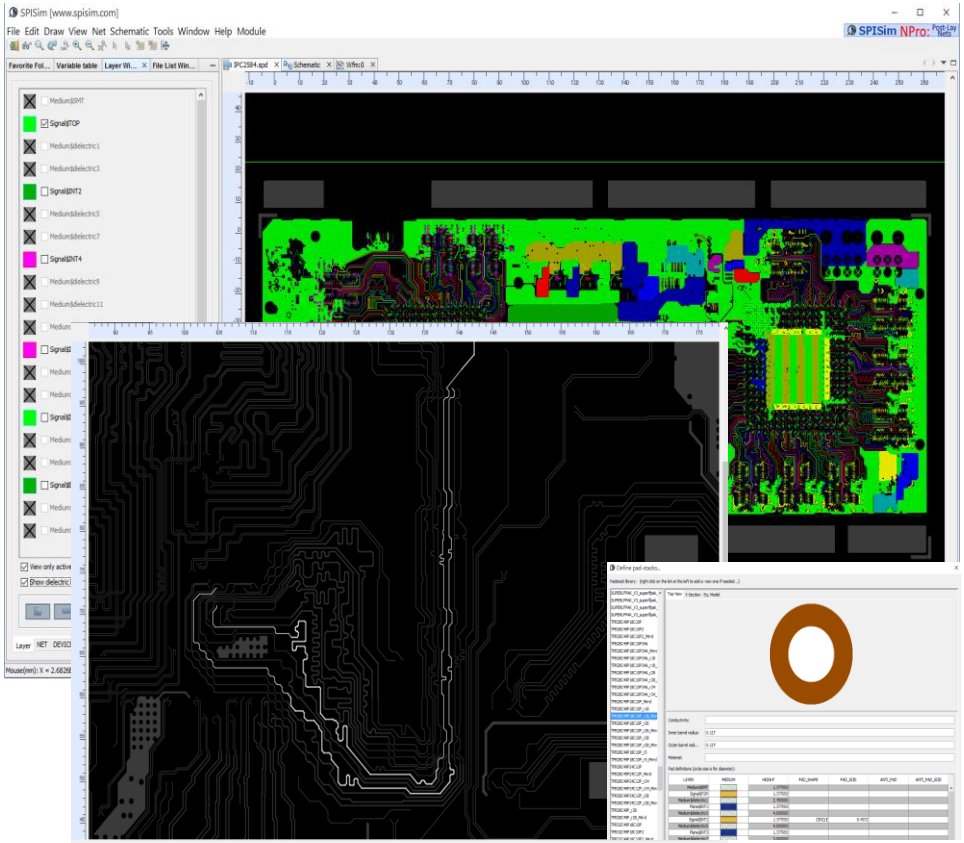
Once design is loaded, user can navigate through different layers, explore nets (nets are sorted by their total length) and generate report such as pin, via and trace components for the selected nets. To mock-up a design, solid or void shapes like polygon, circle and rectangle are supported. User may also add via and traces.

Net extraction:

Before extraction, user may assign pin IBIS models to driver/receiver pins, Pad stack's L/C values and component values such as series resistor and capacitor. Interested net can be selected and highlighted via Net Manager pane. They can be either exported to time domain or frequency domain spice netlist, or schematic to CPro for further analysis.

Design management:

Most of the post-layout design formats are manufacturing centric. Settings such as layer stackup (thickness and material properties), pad-stack (barrel and pad size etc) are back annotated. NPro has simple data management for these info. and settings can be imported/exported for design of next revision.



CPro:

Schematic channel builder and design cockpit

Free form channel builder:

SPICPro provides a system level focused channel builder allowing user to create channel and assign their parameters/models from scratch.

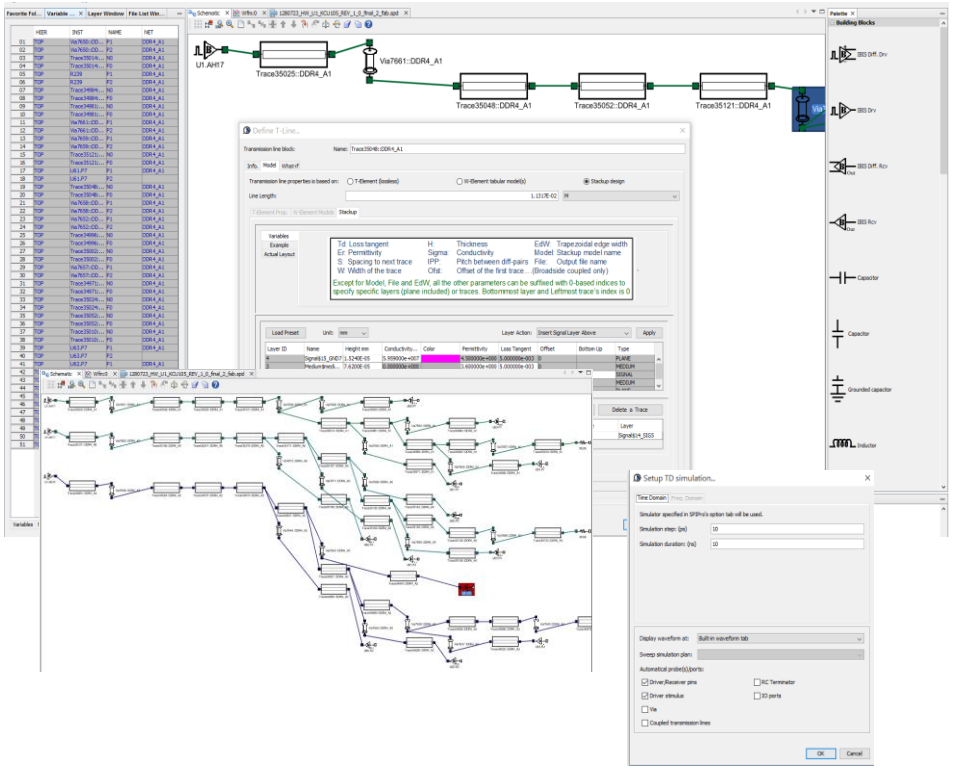
Elements like IBIS, transmission line and s-parameter/sub-circuit are supported and hierarchy is also allowed via sub-circuit. IBIS driver's stimulus can be set-up using SPISim's signal generator module. So USB spec and PRBS like patterns can be assigned directly for interactive or what-if analysis. For transmission line, simple lossless T-element, tabular based W-element and stackup based field solver generated models are all supported.

Net extracted from post-layout:

CPro also enables post-layout net extraction from Npro. Trace segments which are parts of the net will be translated to stackup based transmission line model directly with width and length all setup properly. User can also extract neighboring nets together and define coupling between then using multi-line W-element or stackup based model.

Interactive or what-if analysis:

Composed channel can be exported as time domain spice netlist for bit-by-bit simulation, or frequency domain for s-parameter extraction. HSpice (not included) or compatible simulator is used for simulation. Elements' models can have variables and a what-if simulation plan can be generated using full factorial, space filling or other algorithms. Generated files will be simulated sequentially in CPro and post-processed in other modules such as VPro or DPro.



VPro:

Time domain/Frequency domain waveform viewer

Multi-format waveform viewer:

SPIVPro accept many different data types and formats for analysis. They including TD/FD data like HSpice's tr#/ac# format and comma-separated-value csv (e.g. excel), s-parameters, transmission line tabular table and IBIS model. Large data (>4GB or more) are also support for tr#/ac# and .s#p s-param format.

The following formats are supported for input viewing:

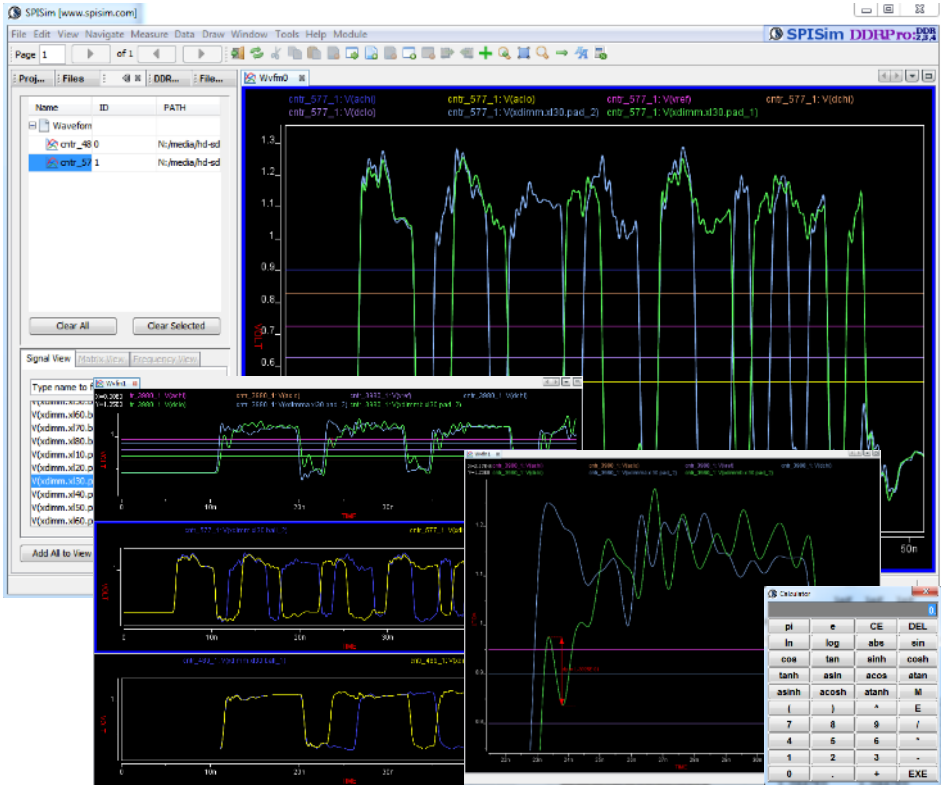
- Synopsys HSpice or ISpice output: .tr#, .ac#, .chi, .split/.spo
- Mentor Graphics Eldo: .swx;
- Matlab: .mat, LTSpice: .raw;
- General csv format from excel, xplot or lab measurement;
- S-param model in .s#p/.ts and .citi;
- Transmission line model in .rlc and .tab;
- IBIS data table up to Spec. V5.1.

Measurement and analysis:

SPIVPro has more than 20 SI focused measurements built-in. These can be used to measure edges, peaks, peak-to-peak or valleys for various SI qualities such as ring-back, overshoot and undershoots etc. Values can be measured across whole x-axis range or specified fixed/moving timing windows. Data measured or peaks/point identified will be marked automatically fir easy reporting.

Waveform calculator/scripting:

SPIVPro has built-in waveform calculator to perform point-to-point calculation between traces and trace groups (like all traces from file A form a group v.s. all traces from file B as a group). Further more, multi-scripting languages such jscript, ruby and tcl are also supported.



SPro:

S-parameter analysis and automation

S-parameter add-on:

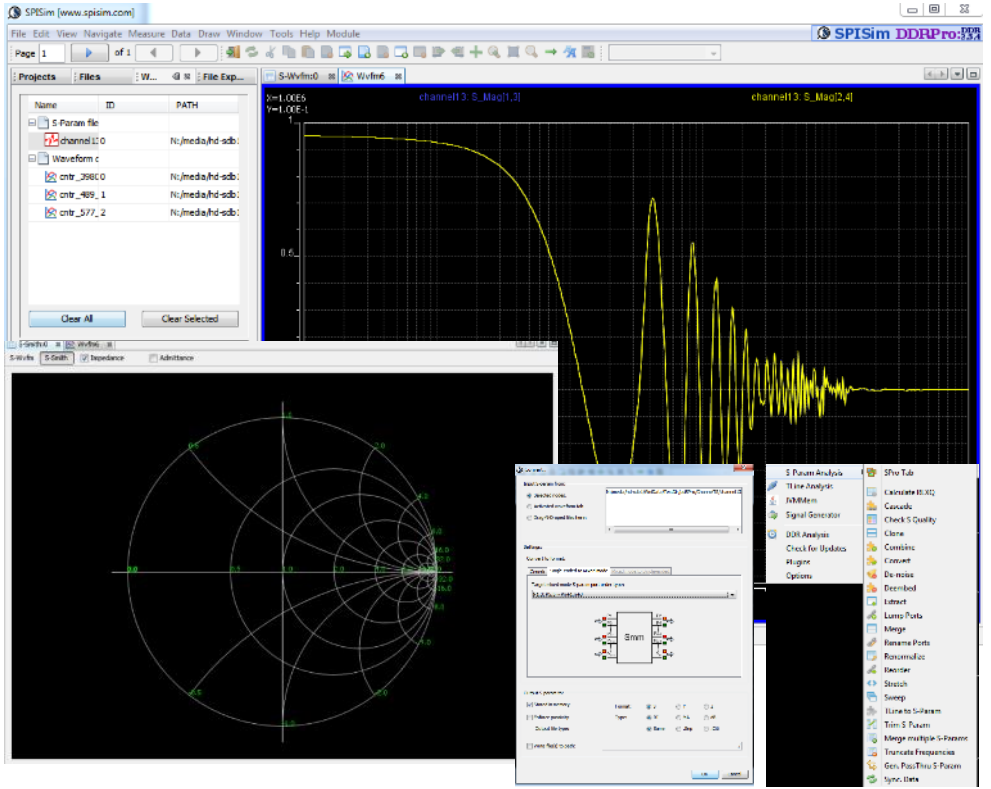
SPISPro is an add-on module on top of SPIVPro waveform viewing/analysis application. It is designed for S-parameters from either simulation or measurement. It supports many S-Param. analysis functions only available at much more expensive EDA tools. Straight-forward UI components targeted at S-Param. also make SI/PI engineers' analysis work with S-Parameters much easier and efficient.

Powerful data viewer:

SPISPro supports both touch-stone (in .s#p/.ts extensions) and citi (.citi) formats. S-Waveform window is an enhanced viewer designed for S-param. data viewing. User can switch between different parameters (S, Y, Z or Mixed-mode etc) with different Y-unit (Magnitude, dB etc) and X-Scale (Linear or Log). Data can be plotted in either trace type viewer or Y/Z Smith-charts. Multi-Pane/Page viewing is also built-in as those are in VPro module. S-Table window enables viewing frequency-specific S-Param. matrix content or frequency-dependent trace value in textual format

Analysis capabilities:

SPro has more than 20 functions like cascade, convert (to mixed-mode or Y/Z), lump ports, re-ordering, renormalizing (to different reference impedance) etc are included. HSpice* input file generation to extract S-Param. via circuit simulation is also supported. A batch processing and reporting function is available to generate summarized report for instant debugging and data analysis.



TPro:

Transmission line modeling and analysis

Transmission-line add-on:

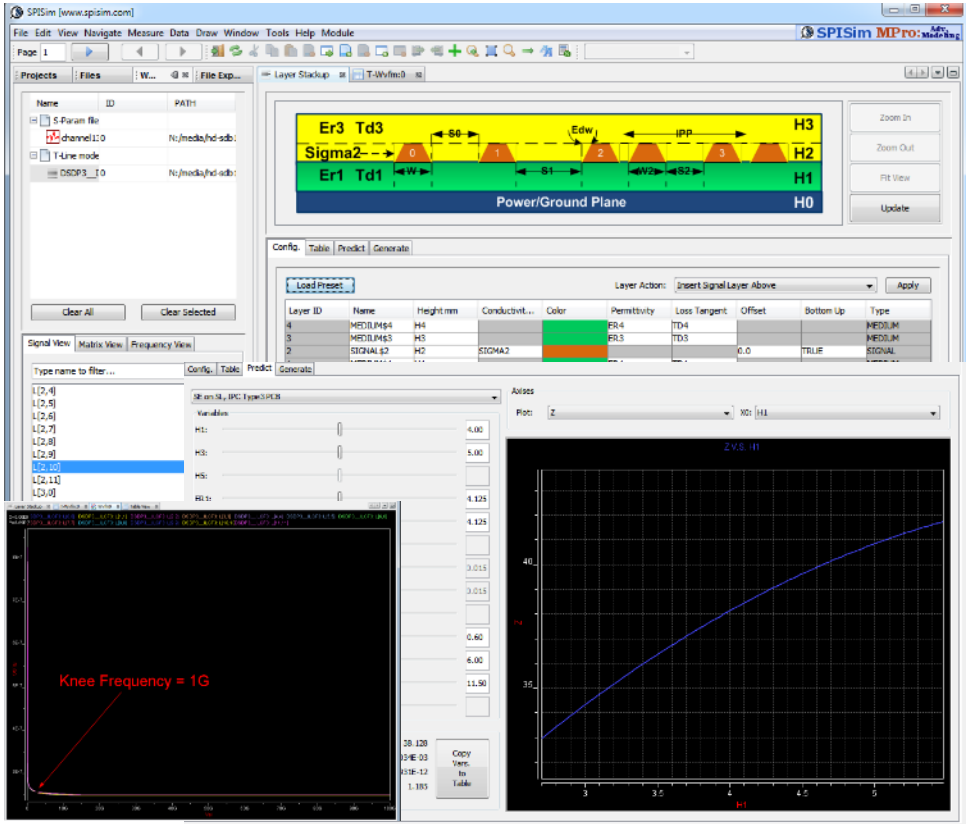
SPITPro is an add-on module on top of SPIVPro waveform viewing/analysis application. It is designed for stackup/transmission which, is an essential portion of platform interconnects. Straight-forward UI components targeted at T-Line models also make SI/PI engineers' analysis work with T-Line modeling/analysis much easier and efficient.

Stack-up analysis/Generation:

SPITPro has a dedicated UI for stackup planer and generation. User can specify predefined or customized stack-up with customized trace conductor layout and their dimension/spacing parameters in tabular format. HSpice* compatible input files will be generated to perform field solving for these input conditions. Generated stackup/T-Line models can then be inspected/checked for their performance qualities such as impedance etc.

T-Line model viewer:

SPITPro supports both parametric (in .rlc extensions) and tabular (.tab) formats. Once activated, SPITPro module will install several extra menu items on-top of VPro menu system. Among which, T-Waveform window is an enhanced viewer designed for T-Line model data viewing. Given a model, user can switch between different views of parameters (impedance, crosstalk, attenuation and propagation speed etc) and X-Scale (Linear or Log). .



MPro:

Modeling and optimization

Sampling creation/collections:

The following sampling methods are provided by SPIMPro: design-of-experiments (DOE), full-factorial, Monte Carlo and custom design. Jscript, Ruby, Python or TCL script may be used to map these generic table into actual input conditions. With built-in pattern replacement functions and multi-threaded execution capabilities, user can create spice input files and perform simulation very efficiently. Post-processed results from these simulation data can then be used for device/system modeling.

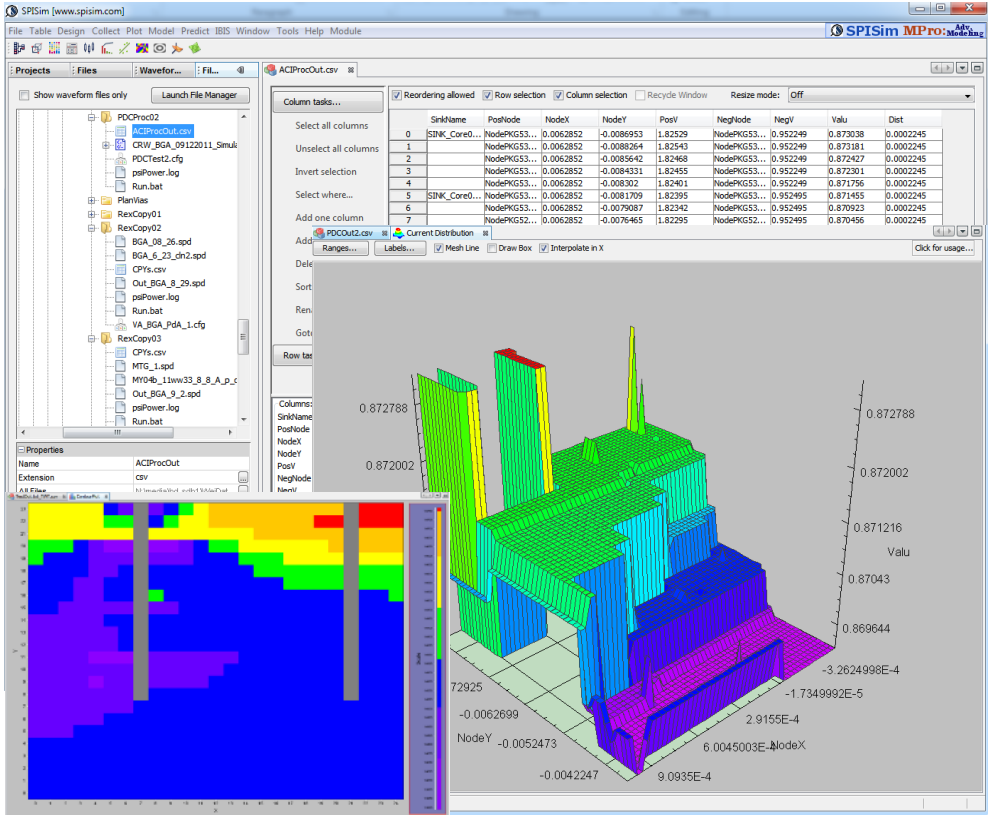
Plot, model and predict:

SPIMPro can plot data points in statistical (distribution, scatter, box-whisker), 2D table (contour and surface) and 3D (stem, contour and surface) plots. It can then normalize the data points or create models using response surface, neural network or wavelet transform. Created models can be exported as HSpice* compatible Verilog-A format or saved for re-evaluation of new data sets.

To evaluate performance or optimize generated models, linear method like linear programming, direct method and non-linear flow like genetic algorithm can be called directly within MPro. Residues and standard-deviation will be calculated and reported either in the table or for plotting.

Table data processing:

SPIMPro supports 10+ table based data processing not available in applications like excel. One may also use SQL to query and filter data sets. MPro has built-in function to convert table into database to facilitate this process.



BPro:

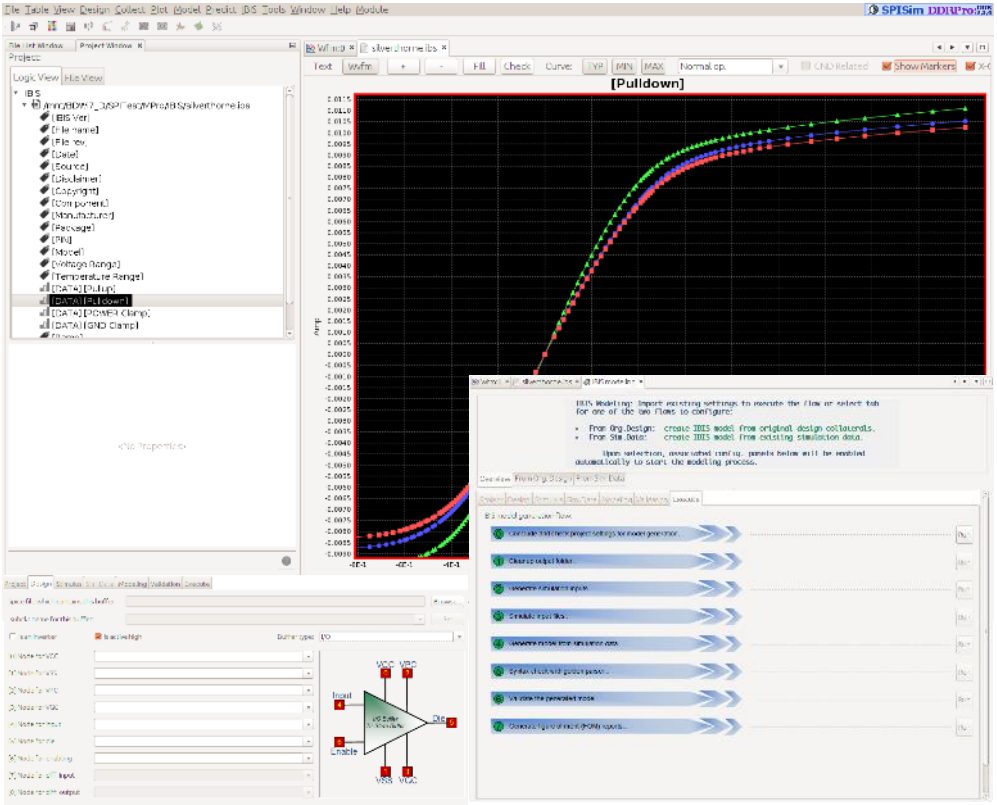
IBIS modeling and analysis

IBIS Modeling from A to Z:

SPIBPro is an add-on flow on SPIMPro for IBIS model inspection, generation, validation and reporting. It can generate IBIS model from either spec. model without simulation, transistor buffer sub-circuit and terminals settings provided or existing buffer simulation results. Step-by-step based full flow will guide user from generate HSpice* compatible input files for test-bench simulations, extract results to generate IBIS models, exercise golden parser to check the syntax/values, and correlate the results to original transistor buffer by validating generated IBIS models and analyze their electrical parameters qualitatively. SPIBPro supports from V3.2 (signal only) to V5.0 (power aware) model generation. It also has fine tuning capability to generate overclockable buffer without sacrificing modeling accuracy.

IBIS model inspector and visualization:

SPIBPro can import IBIS model to cross check texture data and its associated VT/IV/IT data curves. Drop-down menu allow simple switching between different TYP/MIN/MAX corners and VCC/VSS related curves. Convenient in-place data editor allow users to update data point value easily with mouse drag. Multi-pane data viewing allow comparison of IT and VT on the same time axis yet with appropriate voltage/current Y-axis scale. Utility function is available to merge multiple IBIS model files into one easily. Built-in screen capture and powerful editor for capturing data curve and editing modeling data in the same tool.



AMI:

IBIS-AMI modeling and analysis

IBIS AMI Make Easy:

SPISimAMI provides streamlined IBIS-AMI modeling and validation flow within SPIMPro environment. It eliminates the laborours needs to hand code C/C++ AMI functions, compile on different platforms and validate the generated or received AMI models. With SPISimAMI, IBIS-AMI model is streamlined, economical and efficient.

Pre-built AMI IP:

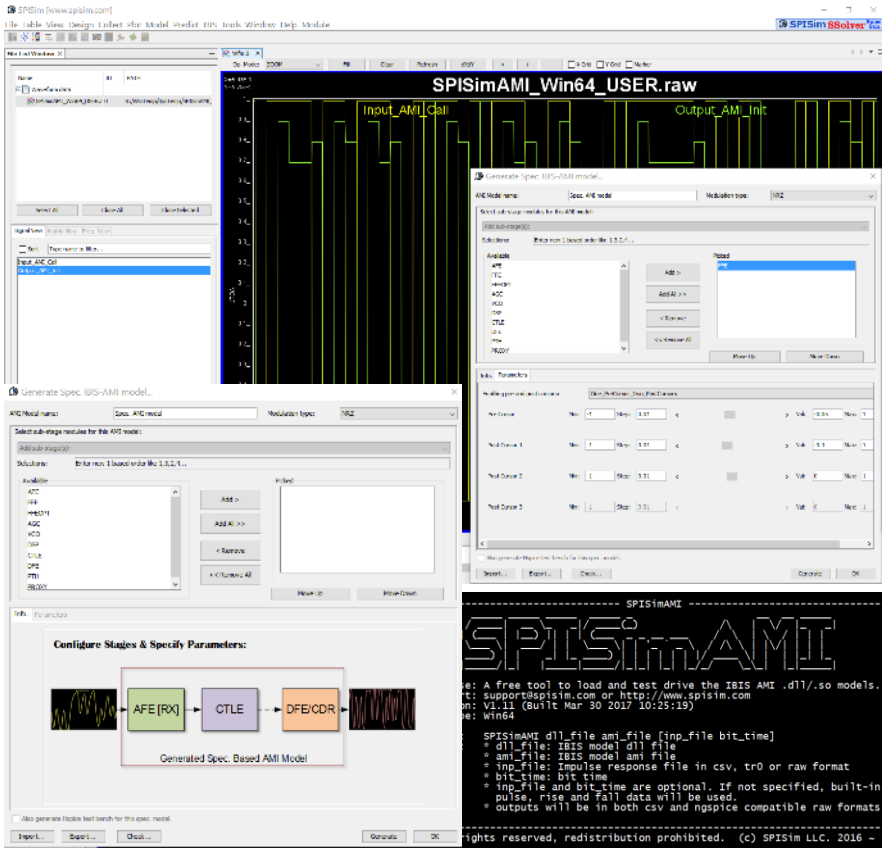
SPISimAMI module has 10+ pre-built analog IPs to support high speed SERDES analyss needs. They include FFE, CTLE, DFE, CDR, Digital Filters, VCO Pulse shaping and more. These modules' functions/performances have been parameterized to allow maximum customization, built with C/C++ and compiled on different platforms for your immediately assembly and use. Frequent AMI usages in common SERDES designs are all covered.

Script based AMI modeling:

When further AMI capabilities are needed, SPISim's script based AMI modeling framework can be used. User will be able to use their most familiar language, such as Matlab, python, perl etc to perform AMI prototyping again without any needs of C/C++ coding or compilation. Encrypted python and direct C-Python embedding is available with add-on features for user to release these model directly with maximum IP protection.

AMI validation:

Integrated environment also provides direct AMI validation using built-in or user provided input stimulus and view results right away.



DPro:

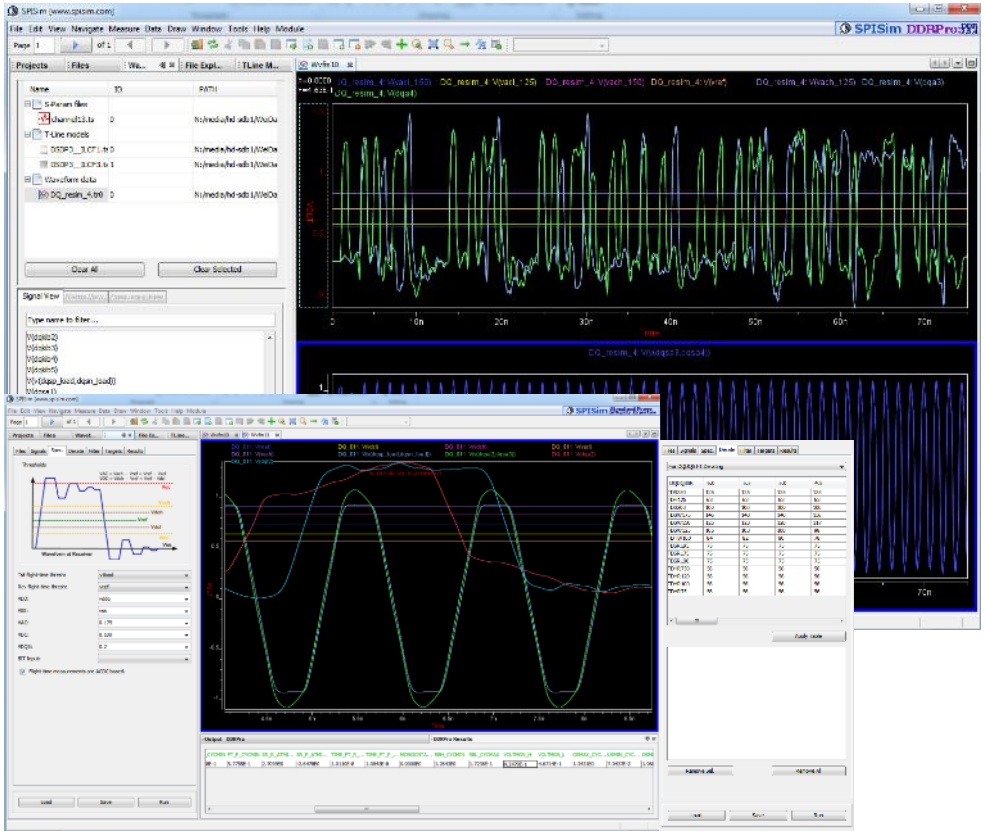
DDR simulation post-processing

DDR data analysis:

SPIDPro is an add-on module on top of SPIVPro waveform viewing/analysis application. It is designed to post-process DDR simulation results. It provides in-place AC/DC derating and report measured results in excel's .csv format. Measurement can be cross-probed to find out the duty cycle in which violation or worst/best case occurred. More than 70 JEDEC compliant measurement can be performed. It comes with pre-defined AC table and also allow user to provide customized table values

Dedicated UI for validation:

Dedicated UI for setup, process and cross validate simulated/measured DDR results. Reported results are cross-referenced to the points where corner case measurement happened. Allowing quick check of results v.s. input data.



EDA Expertise in Signal, Power Integrity and Simulation

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SPISim is a member of Synopsys HSPICE Integrator Program