

SPISim Environment Overview:

With the ever increasing fast data rate in today's system design, a growing percentage of products suffer from signal degradation. Noises such as over/undershoot, ringing, jitter and incorrect setup-hold time caused by impedance/length mismatching may not only decrease the data transmission rate, but also cause system to fail.

Conventionally, hardware engineers and signal integrity specialists alike relies on multiple tools (e.g. solvers, matlab like scripting environments or customized tools) to analyze these signaling issues. While most of the users only utilize very small portion of these tools' capabilities, yet they spend lots of resources (e.g. licensing cost and engineering efforts) to acquire the capabilities and be familiar with the tool usage.

SPISim's products integrates most frequently used signal/power analysis capabilities in a single easy-to-use environment at very reasonable cost. It is to serve most SI/PI engineers' daily tasks' needs and minimize underutilized tool cost.

APPLICATION SCOPES:

- General purpose data analysis, visualization, modeling and optimization.
- IBIS model analysis, generation and validation.
- As a platform for other advanced analog-digital/mixed-signal (AMS) modeling modules.

MAJOR BENEFITS:

- Single integrated environment with all others SPISim's products (e.g. VPro for waveform viewing and analysis), straight-forward UI.
- Support most table based data processing, can convert table to data-base for SQL command search/query.
- Visualize data in various statistical, 2D and 3D plots.
- Model data using response surface modeling, neural network etc. Generate model in HSpice* compatible Verilog-A format for circuit simulation.
- Optimize (Predict best/worst case) using linear, non-linear and genetic algorithm methods.
- Support IBIS modeling via optional add-on. Full modeling flow from test-bench generation, simulation, model generation to validation.

SPIMPro Overview:

To construct a device or system model for performance prediction, many data points are required. Simulations from different input conditions are conducted and post-processed to collect these data points in sampling space. Various modeling algorithms are then used to compute the model. This process is true for either driver/receiver modeling, via/connector or even full channel/system modeling.

SPIMPro product is a modeling tool designed to streamline this modeling process. Built on-top of SPISim framework, it provides an unified, straight-forward environment with many general and advanced analysis capabilities. It supports sampling methods like design-of-experiment, full-factorial or Monte Carlo. Using built-in scripting support and various table based processing capabilities, it can then translate these samplings into various input conditions/spice files for circuit simulation or solving. User can visualize data in different statistical, 2D or 3D plots, construct models with response surface, neural network methods then perform optimization for performance prediction. Constructed model can be exported as Verilog-A models for later evaluation. In addition, it also comes with flow to facilitate IBIS model creations: from test bench set-up generation, simulation, data extraction, golden parser checking to model validation.

With all these features, SPIMpro provides an one-stop shop for all your modeling needs.








Sampling Creation/Collection:

The following sampling methods are provided by SPIMPro: design-of-experiments (DOE), full-factorial, Monte Carlo and custom design. Jscript, Ruby, Python or TCL script may be used to map these generic table into actual input conditions. With built-in pattern replacement functions and multi-threaded execution capabilities, user can create spice input files and perform simulation very efficiently. Post-processed results from these simulation data can then be used for device/system modeling.

Table data processing:

Modeling samples usually comes from different source files, as a table format and in (tens of) thousands of points. Thus, an efficient tool to manipulate and process these table data is a must-have and is also very useful for general data analysis.

SPIMPro supports 10+ table based data processing not available in applications like excel. For example, user can split, stack, transpose, join columns/rows and create statistical summaries for opened tables. One may also use SQL to query and filter data sets. MPro has built-in function to convert table into database to facilitate this process.

	Transpose	Ctrl+K
	Concat	Ctrl+C
	Combine files	
	Join columns	
	Join tables	Ctrl+J
	Update	Ctrl+D
	Query w/ SQL	

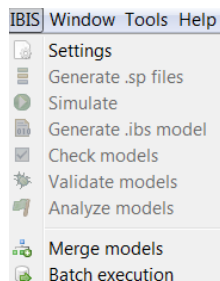
Plot, Model and Predict:

SPIMPro can plot data points in statistical (distribution, scatter, box-whisker), 2D table (contour and surface) and 3D (stem, contour and surface) plots. It can then normalize the data points or create models using response surface, neural network or wavelet transform. Created models can be exported as HSpice* compatible Verilog -A format or saved for re-evaluation of new data sets.

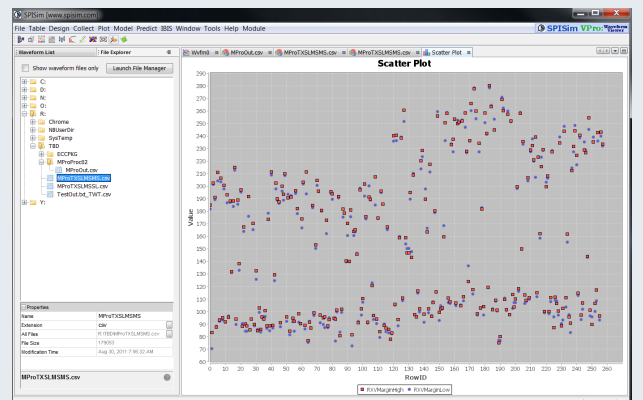
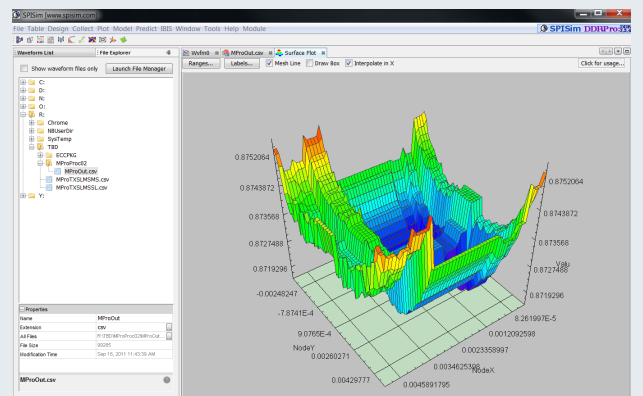
To evaluate performance or optimize generated models, linear method like linear programming, direct method and non-linear flow like genetic algorithm can be called directly within MPro. Residues and standard-deviation will be calculated and reported either in the table or for plotting.

IBIS Model Generation [Add-Ons]:

SPIMPro has a add-on flow for IBIS model generation and validation. With transistor buffer sub-circuit and terminals settings provided, out flow will generate HSpice* compatible input files for test-bench simulations, extract results to generate IBIS models, exercise golden parser to check the syntax/values, and correlate the results to original transistor buffer by validating generated IBIS models and analyze their electrical parameters qualitatively.

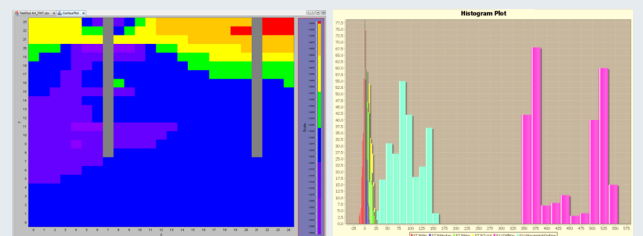


Screenshots:



This screenshot shows a table view in the SPIMPro software, displaying simulation results. The table has columns for 'Voltage', 'I(typ)', 'I(min)', and 'I(max)'. The data is organized into rows, with some rows highlighted in yellow and others in blue.

Voltage	I(typ)	I(min)	I(max)
-9.0000E-1	7.3742E-3	7.1434E-3	8.7334E-3
-8.0000E-1	7.4437E-3	7.2212E-3	8.7808E-3
-7.0000E-1	7.5022E-3	7.2819E-3	8.8142E-3
-6.0000E-1	7.5432E-3	7.3112E-3	8.8338E-3
-5.0000E-1	7.5700E-3	7.3385E-3	8.8507E-3
-4.0000E-1	7.5900E-3	7.4075E-3	8.8441E-3
-3.0000E-1	7.6424E-3	7.4112E-3	8.8912E-3
-2.0000E-1	7.5278E-3	7.4068E-3	8.8503E-3
-1.0000E-1	7.5591E-3	7.3961E-3	8.8996E-3
0.0000E+0	7.4543E-3	7.3874E-3	8.5092E-3
1.0000E-1	7.5865E-3	7.5021E-3	8.7866E-3
2.0000E-1	7.2884E-3	7.5188E-3	8.2658E-3
3.0000E-1	7.2364E-3	7.5021E-3	8.1348E-3
4.0000E-1	7.1860E-3	7.5188E-3	8.1077E-3
5.0000E-1	7.0862E-3	7.7799E-3	8.5666E-3
6.0000E-1	7.0462E-3	7.7799E-3	8.5666E-3
7.0000E-1	6.9324E-3	6.9344E-3	7.7771E-3
8.0000E-1	6.8774E-3	6.8774E-3	7.7771E-3
9.0000E-1	6.7383E-3	6.7494E-3	7.5293E-3
1.0000E+0	6.5836E-3	6.6002E-3	7.1566E-3
1.1000E+0	6.4988E-3	6.5168E-3	7.2346E-3



* SPISim LLC is a member of Synopsys HSPICE Integrator Program. For more info. About HSpice, please visit www.synopsys.com.

<http://www.spisim.com/products/spimpro/>

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